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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
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ART UNIT	PAPER NUMBER
2181	4

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,744	OONO ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) ~~1-68~~ 69 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) ~~1-68~~ 69 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: the serial/patent number and current status of related US Applications cited in pages 15 and 19 of the disclosure must be updated.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claim 46 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 1, "said master bit buckets" lacks antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application

filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-35, 37-46, 48-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Blackmon et al.

At the outset, it is noted that similar claims will be grouped together to avoid repetition in explanation. As broadly drafted, these claims do not define any structure that differs from Blackmon et al.

With regard to claim 37, 38, 42-46, 48, 50-59, and 62-64, Blackmon et al. discloses a processor system comprising: a processor (72, 74, 78); a link hub (42) connected to the processor (72, 74, 78) via a processor bus (104, 106, 108, 110, 116, 118); a satellite device (76, 80, 82); and a link bus (112, 114, 120, 122, 124, 126) connected between the link hub (42) and the satellite device (76, 80, 82), the link bus (42) comprising a status line and a first bus, one of said link hub (42) and said satellite device (76, 80, 83) being a bus master and the other of said link hub (42) and satellite device (76, 80, 83) being a target, wherein said master issues a data transfer request on said first bus, obtains a status of the request by observing said status line during a first predetermined window of time, determines from the obtained request status whether a data transfer corresponding to the request should be initiated, and initiates the data transfer over said first bus when the data transfer should be initiated. Specifically, in Blackmon et al., upon receiving a command or request, each bus device responds by issuing an address status response signal to a response combining logic module or Link Hub (42). The response combining logic module (42) identifies which

bus device (if any) responded to the command or request with a positive acknowledge. The response combining logic module then sends a bus device identifier to the switch via a destination route bus identifying which bus device responded with the positive acknowledge. The switch uses the device identifier returned via the response combining logic to route any subsequent data transfers associated with the issued command or request. FIG. 1 shows a plurality of bus devices 32A, 32B, 32C and 32D, hereinafter referred to collectively as 32, connected to a centralized switch 34 via a plurality of point-to-point connections 36A, 36B, 36C and 36D, hereinafter referred to collectively as 36. Bus devices 32 include, but are not limited to: processors, I/O hubs, and memory controllers. The plurality of point-to-point connections 36 collectively form a system bus for the switch based topology. A response combining logic module or Link Hub 42 is coupled to each bus device 32 via address status response signals 37A, 37B, 37C and 37D, hereinafter referred to collectively as 37. Address status response signals 37 carry a signal response generated by each of the bus devices 32 in response to an issued command or request on the system bus. See also Table 1 and description thereof. Also shown in Fig. 1, for each address bus 38 operation there are three major points where information can be passed. The address command is always the first point, where a bus master drives address bus 38. The second point where information is passed in the address status mechanism occurs when bus devices 32 provide low latency feedback (two-bit address status output (AStatOut) signal and a two-bit address status input (AStatin) signal) in response to the issued command or request. The AStatOut/AStatIn status response signals 37 provide a positive acknowledge of an

address being accepted by a bus device, a null response (stall), or an indication that the transaction should be terminated immediately (i.e., address parity error or retry). A slave drives the AStatOut signal(s) active starting on the second cycle after it samples an address, and holds the AStatOut signal(s) active for two clock cycles (or a so-called "a first predetermined window of time." The address status AStatIn is typically sampled 2 bus clock cycles later. Alternatively, the signals may be latched and re-driven after one additional bus clock cycle. AStatOut and AStatIn are then driven anew if a new address cycle is begun, or inactivated. AStatOut and AStatIn are always driven. In another word, data transfer can always be retried (if "stall" occurs) in every or a predetermined number of predetermined clock cycle(s), namely first, second, third "predetermined window of time." With regard to claim 38, in Blackmon et al., the bus identifier identifies which of the plurality of bus devices returned the positive acknowledge to the issued command; and routing a data packet associated with the issued command to the bus device returning the positive acknowledge response to the issued command (see claim 8 of Blackmon et al.). With regard to claims 39-41, 60, and 61, in Blackmon et al., when a requestor issues a request, a bus master drives the address portion with an address, an operation type identifier which defines a particular operation using the address bus, and the size of any data transferred as a result of the transaction. The address also includes an 8-bit address tag which is used to identify the operation to a particular master and command instance. With regard to claim 49, it is clear from the data transfer protocol disclosed by Blackmon et al. and also, from the discussion above that the transfer should be stopped when such transfer is on a

boundary of data. With regard to claims 1-35, one using the device of Blackmon et al. would have performed the same steps set forth in claims 1-35.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon et al.

Blackmon et al. discloses the claimed invention except the use of a pull-up resistor for driving the request or command status onto the request line. However, such pull-up resistor is old and well-known as evidenced from Kim et al. and Edwards et al., both cited below as supportive evidences. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Blackmon et al. with a pull-up resistor for driving the request or command status onto the request line of Blackmon et al., since the Examiner takes Official Notice that such pull-up resistor is old and well-known for its use to drive the request status to a request line as clearly evidenced from at least Kim et al. and Edwards et al.

Claims 65 and 66, 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon et al.

Blackmon et al. discloses the claimed invention including the use of address bus 38 having 64 bits wide for supporting addressing of multiple address spaces. For example, the multiple address spaces may include a multiple microchannel I/O space of 32 bits, a real memory space of 48 bits maximum, and a special purpose address space to pass interrupts and processor commands between bus devices 32. Address bus 38 includes an address tag used to identify the current operation to a particular Master and command instance. This tag is matched with a corresponding tag on data bus 40 at switch 34 to associate any data that corresponds to this address command. Blackmon et al. does not disclose the use of a time multiplexor, as an alternative way for either initiating, disconnecting, retry, aborting and stalling data transfer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Blackmon et al. with such a time multiplexing device, as an alternative way, to either initiate, disconnect, retry, abort and stall data transfer, since the Examiner takes Official Notice that such time multiplexing device is old and well know and using one to implement a function of logically initiating, disconnecting, retry, abort and stall, for example, is clearly within level of one having ordinary skill in the art. If Applicants choose to challenge the fact that such time multiplexer is old and well-known for the purpose discussed above, supportive evidences will be provided upon request.

Claims 66 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon et al.

The further difference between Blackmon et al. and the claimed subject matter is the use of a pull-up resistor for driving the request or command status onto the request line. However, such pull-up resistor is old and well-known as evidenced from Kim et al. and Edwards et al., both cited below as supportive evidences. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Blackmon et al. with a pull-up resistor for driving the request or command status onto the request line of Blackmon et al., since the Examiner takes Official Notice that such pull-up resistor is old and well-known for its use to drive the request status to a request line as clearly evidenced from at least Kim et al. and Edwards et al.

US Patent Nos. 6,463,092 to Kim et al., 6,530,047 to Edwards et al., 6,279,064 to Bronson et al., 5,101,478 to Fu et al., and 6,073,186 to Murray et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner